AP-706

APPLICATION NOTE

DRAM Controller for 40 MHz i960® CA/CF Microprocessors

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DRAM CONTROLLER FOR 40 MHZ I960® CF MICROPROCESSORS

FIGURES

TABLES

1.0 INTRODUCTION

This application note describes a DRAM controller for use with the i960® CF 40 MHz microprocessor. Other application notes are available which describe DRAM controllers for the i960 Cx and Jx processors; see Section 7.0, RELATED INFORMATION for ordering information.

This DRAM controller's design features include:

- Interleaved design
- Can use standard 70 ns DRAM SIMM
- 4-0-1-0/3-0-1-0 back-to-back/idle bus wait state burst reads up to 40 MHz
- 3-1-1-1/2-1-1-1 back-to-back/idle bus wait state burst writes up to 40 MHz
- Single clock input to state machines

This document contains some general DRAM controller theory as well as this design's state machine definitions and timing diagrams. It also contains the PLD equations used to build and test the prototype design. All timing analysis was verified with Timing Designer*. PLD equations were generated in ABEL* as a device-independent design. Schematics were created in OrCAD*. The timing analysis, schematics and PLD files are available through Intel's America's Application Support BBS, at (916) 356-3600.

2.0 OVERVIEW

This section provides an overview of DRAM SIMM operation and the concept of memory interleaving. It also describes the i960 Cx microprocessor burst capabilities.

2.1 Page Mode DRAM SIMM Review

Page mode DRAM allows faster memory access by keeping the same row address while selecting random column addresses within that row. A new column address is selected by deasserting $\overline{CAS}$ while keeping $\overline{RAS}$ active and then asserting $\overline{CAS}$ with the new column address valid to the DRAM. Page mode operation works very well with burst buses in which a single address cycle can be followed by multiple data cycles.

All $\overline{WE}$ pins on each SIMM are tied to a common $\overline{WE}$ line; this line requires the use of early write cycles. In an early write cycle, write data is referenced to the falling edge of $\overline{CAS}$, not the falling edge of $\overline{WE}$.

Each SIMM also has four $\overline{CAS}$ lines, one for every eight (nine) bits in a 32-bit (36-bit) SIMM module. The four $\overline{CAS}$ lines control the writing to individual bytes within each SIMM.

2.2 Bank Interleaving

Interleaving significantly improves memory system performance by overlapping accesses to consecutive addresses. Two-way interleaving is accomplished by dividing the memory into two 32-bit banks (also referred to as "leaves"):

- one bank for even word addresses (A2=0)
- one bank for odd word addresses (A2=1)

The two banks are read in parallel and the data from the two banks is multiplexed onto the processor's data bus. This overlaps the wait states of:

- the second access with the first
- the third access with the second
- the fourth access with the third

Figure 1 shows DRAM with a 2-1-1-1 quad word burst read wait state profile being interleaved to generate a 2-0-0-0 wait state system.

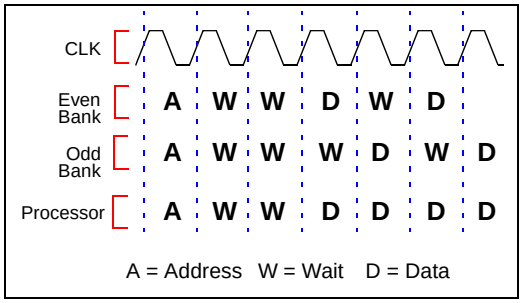

Figure 1. Two-Way Interleaving

2.3 Burst Capabilities for 32-Bit Bus

A bus access starts by asserting $\overline{ADS}$ in the address cycle, and ends by asserting $\overline{BLAST}$ in the last data cycle. Figure 2 shows $\overline{ADS}$ and $\overline{BLAST}$ timings for a quad-word access. i960 Cx processor's burst protocol requires:

- Quad-word and triple-word requests always start on quad word boundaries (A3 = 0, A2 = 0).
- Double-word requests always start on double word boundaries (A3 = X, A2 = 0).

- Single-word requests can start on any word boundary (A3 = X, A2 = X).
- Any request starting on an odd word boundary will never burst (A3 = X, A2 = 1).

3.0 DRAM CONTROLLER OVERVIEW

Figure 3 shows a block diagram of the DRAM Controller. The DRAM controller comprises four distinct blocks: control logic, address path, data path, and the DRAM SIMMS. This section describes each block.

3.1 Control Logic

The DRAM controller is centered around a four-bit state machine which controls DRAM bank accesses and refreshing. All timings are generated based on the four-bit state machine's outputs. Some states are used for both read and write accesses. The state machine uses the W_$\overline{R}$ signal from the processor to distinguish between reads and writes. This technique allows the state machine to use fewer states; therefore, fewer output bits.

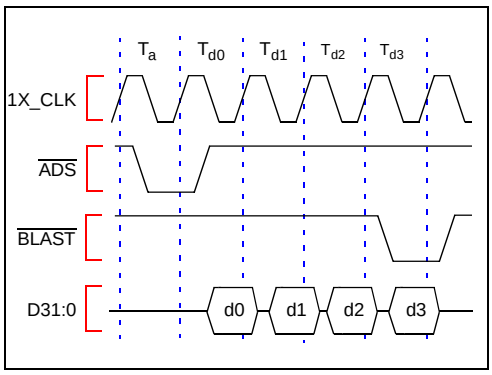

Figure 2. Quad-Word Access Example Showing $\overline{ADS}$ and $\overline{BLAST}$ Timings

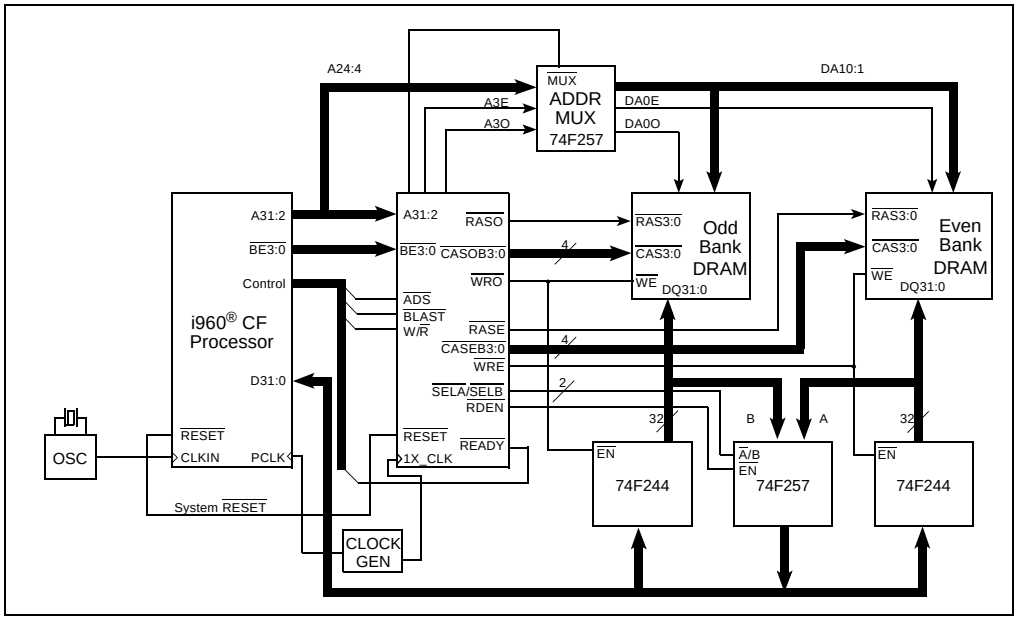

Figure 3. DRAM Controller Block Diagram

3.1.1 Refresh Logic

Typically DRAMs need to be refreshed every 15.6 µs. In this design, due to power requirements needed to refresh an entire DRAM array, one bank is refreshed at a time. The DRAM controller uses an eight-bit counter to generate refresh requests. A refresh request is generated every 7.8 µs. The DRAM controller toggles between refreshing each bank every 7.8 µs which means each bank is effectively refreshed every 15.6 µs.

A refresh request has priority over a processor request. When a processor and a refresh request occur simultaneously, the DRAM controller sequences a refresh to the appropriate DRAM bank while the PENDING state machine posts the processor request. The pending request is then serviced after the refresh is completed.

An eight-bit synchronous down counter is used to generate refresh requests. The counter is clocked using the 1X_CLK clock. The $\overline{\text{REFREQ}}$ signal is asserted each time the counter reaches zero. Counting is inhibited when the counter reaches zero. The counter is reloaded with 0xff and counting resumes after the ACCESS state machine services the refresh. During reset, the counter is loaded with 0xff.

3.1.2 Clock Generation

A Motorola* MC88915 low skew CMOS PLL generates the clock signals for the DRAM controller. The MC88915 uses PCLK2 as an input, and produces four very low skew copies of PCLK2, as well as a 2x PCLK. At 40 MHz, the maximum skew between PCLK2 and any of the MC88915 outputs was calculated to be ±1 ns, while the skew between any of the individual outputs is ±750 ps under equal loading conditions. All clock lines are terminated with 22 ohm series resistors.

3.1.3 Wait State Profile

The DRAM Controller uses the processor's $\overline{\text{READY}}$ signal to control wait states. The MCON register is initialized as follows: (N_{XAD} = N_{XDA} = N_{XDD} = N_{XDA} = 0). Table 1, Wait State Profiles, provides the wait state profiles for read and write accesses up to 40 MHz.

Back-to-back accesses require an extra wait state to meet RAS precharge time. Therefore, to meet the RAS precharge time required, the first data access for reads uses four wait state cycles as opposed to three wait state cycles for idle bus DRAM accesses. For writes, the first data access uses three wait state cycles for back-to-back accesses, as opposed to two wait state cycles for idle bus.

Table 1. Wait State Profiles (40 MHz)

Access Type	Wait State Profile	
	Back-To-Back	*Idle Bus*
Quad Word Read	4-0-1-0	3-0-1-0
Triple Word Read	4-0-1	3-0-1
Double Word Read	4-0	3-0
Single Word Read	4	3
Quad Word Write	3-1-1-1	2-1-1-1
Triple Word Write	3-1-1	2-1-1
Double Word Write	3-1	2-1
Single Word Write	3	2

3.2 Address Path

Figure 4 illustrates a block diagram of the address path logic. The 2-to-1 multiplexers combine the row and column addresses into a singular row/column address that the DRAM requires. DA0E and DA0O equivalent signals are generated, one for each bank. DA0E and DA0O are generated by using A3E and A3O respectively. DA0E and DA0O are the only address bits that increment during bursts. The timing of these signals during bursts is critical for proper operation.

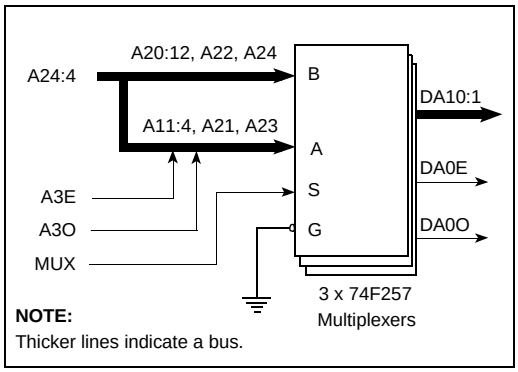

Figure 4. Address Path Logic

3.3 Data Path

As shown in Figure 5, there is one data path for reads and a separate data path for writes. The read path uses 74F257 2:1 multiplexers to prevent contention between the two DRAM banks. $\overline{CAS}$ can be active for both banks at the same time, necessitating use of the multiplexers. The multiplexer outputs are enabled only during reads by the $\overline{RDEN}$ signal. The multiplexers are switched using $\overline{SELA}$ and $\overline{SELB}$. These signals are derived based on the states of the ACCESS state machine and address A2. The write data path consists of eight 8-bit 74F244 buffers, four for each bank. The buffer outputs are enabled by $\overline{WRE}$ and $\overline{WRO}$.

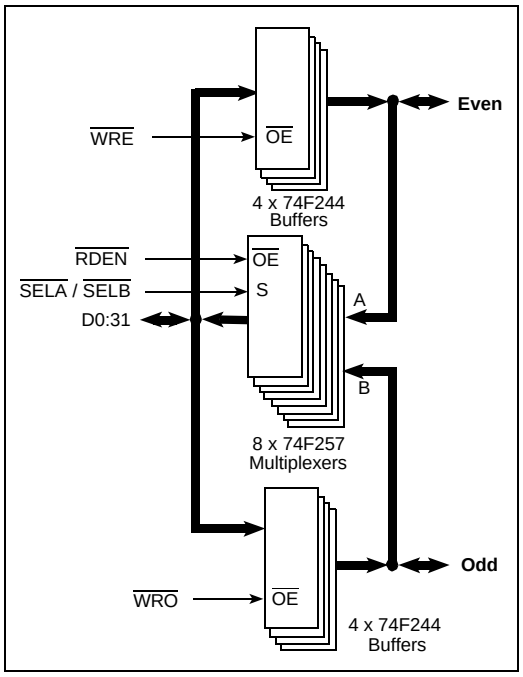

Figure 5. Data Path Logic

3.4 SIMMS

The SIMM block consists of two standard 72-pin SIMM sockets, arranged as two banks: odd and even. The x36 SIMM parity bits are not used in this design. The x36 SIMMs are standard for PCs and workstations, which makes them readily available. The only penalty is more address and control line loading due to the extra DRAM devices of the x36 SIMM. All address and control lines to the SIMMs are terminated with 22 ohm resistors.

4.0 STATE MACHINES AND SIGNALS

This section describes the state machines and signals used in this design. Most of the state machines are simple and the PLD equations can be referenced in APPENDIX A. The ACCESS state machine is the most complex of all the state machines; for that reason, this application note provides more detail on the operations of this state machine. In this design, all the state machines are clocked using 1X_CLK clock (bus clock).

All PLD equations are written in ABEL. APPENDIX A, PLD EQUATIONS contains a listing of the PLD equation file. The state machine transitions described here follow the ABEL conventions for logic operators.

- ! represents NOT, bit-wise negation
- & represents AND
- # represents OR

To follow the ABEL conventions, active LOW signals (such as ADS) already have a polarity assigned. For example, in the state machines, ADS refers to the asserted state (LOW) and !ADS refers to the non-asserted state (HIGH).

4.1 ACCESS State Machine

The ACCESS state machine, the “heart” of the DRAM controller, is implemented as a four-bit state machine. See Figure 6, Basic ACCESS State Machine. It is responsible for sequencing accesses as well as refreshes to the DRAM banks.

From the IDLE state, the access state machine is sequenced based on these three events:

- Refresh requests from the counter
- DRAM requests from the processor
- PENDING state machine requests

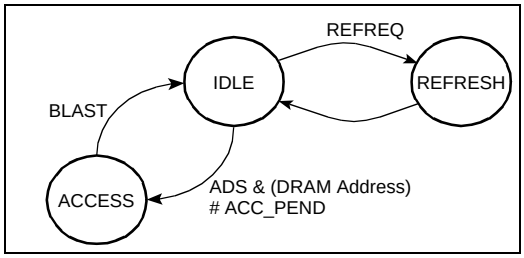

Figure 6. Basic ACCESS State Machine

4.2 PENDING State Machine

The PENDING state machine is a one-bit state machine which monitors DRAM requests from the processor. This is necessary because a DRAM refresh has priority over a processor request. Therefore, this state machine is used to post the processor request. The state machine gets reset once the ACCESS state machine starts sequencing the pending request. The state machine generates $\overline{\text{ACC\_PEND}}$.

4.3 ODDACCESS State Machine

The ODDACCESS state machine is clocked using the 1X_CLK clock. It is a one-bit state machine which monitors the initial state of the processor's address A2. Several state machines in this design use the output of this state machine as inputs. Address A2 from the processor indicates whether an access starts on an even or odd word boundary. The ACCESS state machine uses this bit extensively. It is important to latch address A2 because the processor toggles address A2 on burst accesses. This state machine generates $\overline{\text{LA2}}$.

4.4 BANKSELA State Machine

The BANKSELA state machine is a one-bit state machine which is used to control the data multiplexer, primarily to select between even or odd data during read accesses. This state machine is clocked using the 1X_CLK clock. It generates $\overline{\text{SELA}}$.

4.5 BANKSELB State Machine

The BANKSELB state machine is a one-bit state machine which is used to control the data multiplexer, primarily to select between even or odd data during read accesses. This state machine is clocked using the 1X_CLK clock. It generates $\overline{\text{SELB}}$.

4.6 ADDRMUX State Machine

The ADDRMUX state machine is a one-bit state machine which is used to control the address multiplexers, primarily to select between row or column addresses. It is clocked using the 1X_CLK clock. This state machine generates $\overline{\text{MUX}}$, which is a delayed version of $\overline{\text{RASE}}$. By delaying the switching of the row address by one 1X_CLK clock cycle provides ample row address hold time (t_{RAH}) required by the DRAM. The row address is selected while $\overline{\text{MUX}}$ is high; otherwise, the column address is selected.

4.7 A3EVEN State Machine

The A3EVEN state machine is a one-bit state machine which is toggled on burst accesses to select the next data word (next column data). The state machine is initially loaded with the value of the processor's address A3 and then toggled for the next data access. This state machine is clocked using 1X_CLK clock, and generates A3E. This signal is an input to the address multiplexer.

4.8 A3ODD State Machine

The A3ODD state machine is a one-bit state machine and has the same functionality as the A3EVEN state machine. This state machine generates A3O.

4.9 RFEVENBK State Machine

The RFEVENBK state machine is a one-bit state machine which is used to indicate which of the two banks (even or odd) to refresh. The two banks are refreshed separately. The even bank is refreshed when the RFEVENBK state machine is active; otherwise, the odd bank is refreshed. The output of this state machine is toggled on every refresh. This state machine generates $\overline{\text{REFEVEN}}$.

4.10 CASPIPE State Machine

The CASPIPE state machine is a one-bit state machine which generates a pipelined $\overline{\text{CAS}}$ signal one 1X_CLK clock cycle earlier. The output of this state machine is then fed to the CASE_B3:0 state machines where it is reconstructed to drive the $\overline{\text{CAS}}$ lines of the even bank. This state machine generates $\overline{\text{CASEE}}$.

4.11 CASPIPO State Machine

The CASPIPO state machine is a one-bit state machine which generates a pipelined $\overline{\text{CAS}}$ signal one 1X_CLK clock cycle earlier. The output of this state machine is then fed to the CASO_B3:0 state machines where it is reconstructed to drive the $\overline{\text{CAS}}$ lines of the odd bank. This state machine generates $\overline{\text{CASOO}}$.

4.12 CASE_B3:0 State Machines

The CASE_B3:0 state machines control the $\overline{\text{CAS}}$ pins of the even bank. CASEB0 controls the least significant byte and $\overline{\text{CASEB3}}$ controls the most significant byte. The CASE_B0 state machine generates $\overline{\text{CASEB0}}$, and the CASE_B3 state machine generates $\overline{\text{CASEB3}}$. $\overline{\text{CASEB0}}$ is

asserted when $\overline{\text{CASEE}}$ and the processor's $\overline{\text{BE0}}$ signal are asserted. $\overline{\text{CASEB3}}$ is asserted when $\overline{\text{CASEE}}$ and the processor's $\overline{\text{BE3}}$ signal are asserted. CASE_B3:0 state machines are clocked using the 1X_CLK clock.

4.13 CASO_B3:0 State Machines

The CASO_B3:0 state machines control the $\overline{\text{CAS}}$ pins of the odd bank. CASO_B0 controls least significant byte and CASO_B3 controls the most significant byte. The CASO_B0 state machine generates $\overline{\text{CASOB0}}$, and the CASO_B3 state machine generates $\overline{\text{CASOB3}}$. $\overline{\text{CASOB0}}$ is asserted when $\overline{\text{CASOO}}$ and the processor's $\overline{\text{BE0}}$ signal are asserted. $\overline{\text{CASOB3}}$ is asserted when $\overline{\text{CASOO}}$ and the processor's $\overline{\text{BE3}}$ signal are asserted. The CASO_B3:0 state machines are clocked using the 1X_CLK clock.

4.14 $\overline{\text{REFREQ}}$ Signal

$\overline{\text{REFREQ}}$, an active low signal, is the output of an eight-bit counter. The counter is clocked using the 1X_CLK clock. $\overline{\text{REFREQ}}$ is asserted when the counter reaches zero. The ACCESS state machine uses $\overline{\text{REFREQ}}$ to sequence refreshes.

4.15 RASEVEN State Machine

The RASEVEN state machine is a one-bit state machine which is used to generate $\overline{\text{RAS}}$ signals for the even bank. It is clocked using the 1X_CLK clock. This state machine generates $\overline{\text{RASE}}$.

4.16 RASODD State Machine

The RASODD state machine is a one-bit state machine which is used to generate $\overline{\text{RAS}}$ signals for the odd bank. It is clocked using the 1X_CLK clock. This state machine generates $\overline{\text{RASO}}$.

4.17 $\overline{\text{SRASE}}$ State Machine

The SRASE state machine is a one-bit state machine which is used to monitor back-to-back DRAM accesses. It is generated by shifting $\overline{\text{RASE}}$ by one 1X_CLK clock cycle. This state machine generates $\overline{\text{SRASE}}$. By using the state of this signal the DRAM controller can eliminate one wait state cycle for accessing the first data word. Back-to-back accesses require an extra wait state cycle to satisfy the RAS precharge time (t_{RP}).

4.18 $\overline{\text{RDEN}}$ Signal

$\overline{\text{RDEN}}$ is asserted while a DRAM read is in progress. It controls the output enables of the data multiplexers.

4.19 $\overline{\text{WRE}}$ Signal

$\overline{\text{WRE}}$ is asserted while a DRAM write is in progress. It controls the even leaf $\overline{\text{WE}}$ lines to perform early writes. It also controls the even data path buffers output enables.

4.20 $\overline{\text{WRO}}$ Signal

$\overline{\text{WRO}}$ is asserted while a DRAM write is in progress. It controls the odd leaf $\overline{\text{WE}}$ lines to perform early writes. It also controls the odd data path buffers output enables.

5.0 DRAM CONTROLLER ACCESS FLOW

This section explains how the ACCESS state machine is sequenced while reading, writing, and refreshing DRAMs. Examples used are:

- quad-word read
- single-word read
- quad-word write
- single-word write
- refresh

The examples in this document assume back-to-back DRAM accesses or pending accesses. For example, the first data access of a DRAM request uses four wait states for reads and three wait states for writes. For idle bus accesses, the ACCESS0 state is skipped, allowing only three wait states for reads and two wait states for writes. Refer to the PLD equations in APPENDIX A. The ACCESS state machine uses $\overline{\text{SRASE}}$ to detect back-to-back accesses.

$\overline{\text{RDEN}}$ is asserted during read accesses while $\overline{\text{WRE}}$ and $\overline{\text{WRO}}$ are asserted during write accesses.

5.1 Quad-Word Read

Figure 7 shows the state diagram for a quad-word read; Figure 8 shows the timing diagram. This state diagram also shows the state machine paths for triple-, double-, and single-word reads. Single-word reads which are aligned on odd word boundaries use a different path; therefore, a separate example is used to explain that state machine path.

From the IDLE state, the machine enters the ACCESS0 state due to a processor request or a pending processor request. At the end of the IDLE state, the A3EVEN and A3ODD state machines are loaded with the processor's address A3 and the ODDACCESS state machine is loaded with the processor's address A2. While in the IDLE state, $\overline{MUX}$ is deasserted, which selects the row address.

At the end of the ACCESS0 state, the $\overline{RASE}$ and $\overline{RASO}$ are asserted. The machine then proceeds to the ACCESS1 state.

At the end of the ACCESS1 state, $\overline{MUX}$ is asserted. This causes the column address to be selected. $\overline{CASEE}$ is asserted, and the PENDING state machine is reset. From ACCESS1, the machine enters ACCESS2 state.

At the end of the ACCESS2 state, $\overline{CASEB}$3:0 are asserted if $\overline{CASEE}$ and the respective Byte Enable signals from the processor are asserted. $\overline{CASOO}$ is asserted if $\overline{BLAST}$ is not asserted. The machine then proceeds to the ACCESS3 state.

At the end of the ACCESS3 state, $\overline{CASOB}$3:0 are asserted if $\overline{CASOO}$ and the respective Byte Enable signals from the processor are asserted, while $\overline{CASEE}$ is deasserted. The machine then proceeds to the ACCESS4 state.

The ACCESS4 state is the first or third data cycle (T_{d0}/T_{d2}) for read accesses aligned on even word boundaries. At the end of ACCESS4, $\overline{CASEE}$ is reasserted while $\overline{CASEB}$3:0 are deasserted. $\overline{CASEB}$3:0 are deasserted because $\overline{CASEE}$ is sampled deasserted. $\overline{CASOO}$ is deasserted before leaving this state. From here, the machine can proceed to either the ACCESS5 or the IDLE state. If $\overline{BLAST}$ is asserted, the machine proceeds to the IDLE state; otherwise, to the ACCESS5 state.

The ACCESS5 state is the second or fourth data cycle (T_{d1}/T_{d3}) for read accesses. At the end of the ACCESS5 state, $\overline{CASOO}$ is reasserted. $\overline{CASEB}$3:0 are asserted if $\overline{CASEE}$ and the respective Byte Enable signals from the processor are asserted. $\overline{CASOB}$3:0 are deasserted because $\overline{CASOO}$ is sampled deasserted. From here, the machine can proceed to either the ACCESS3 or the IDLE state. If $\overline{BLAST}$ is asserted, the machine proceeds to the IDLE state; otherwise, to the ACCESS3 state. The machine then proceeds to ACCESS3 state.

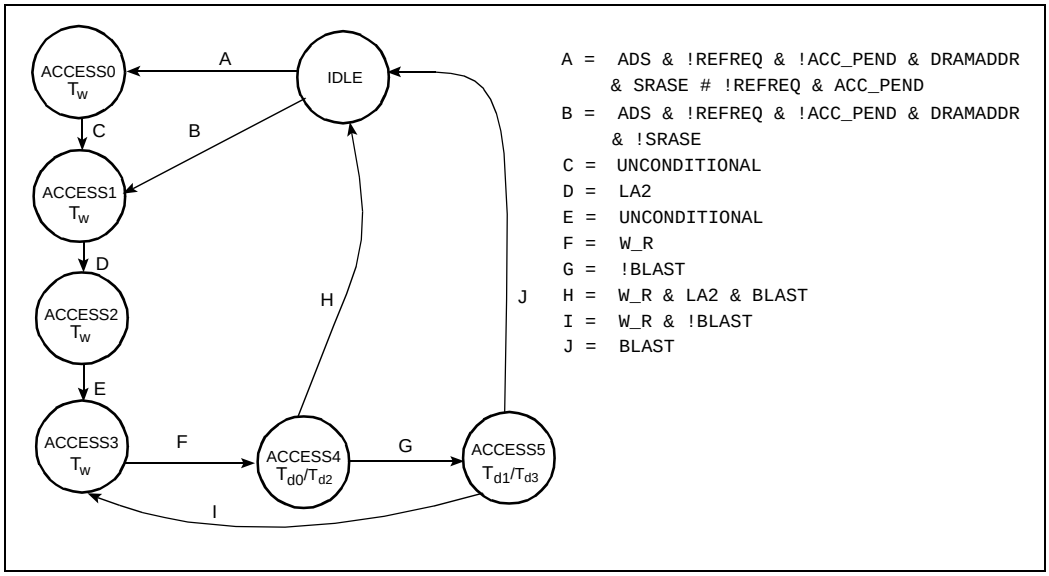

Figure 7. Quad-Word Read State Diagram

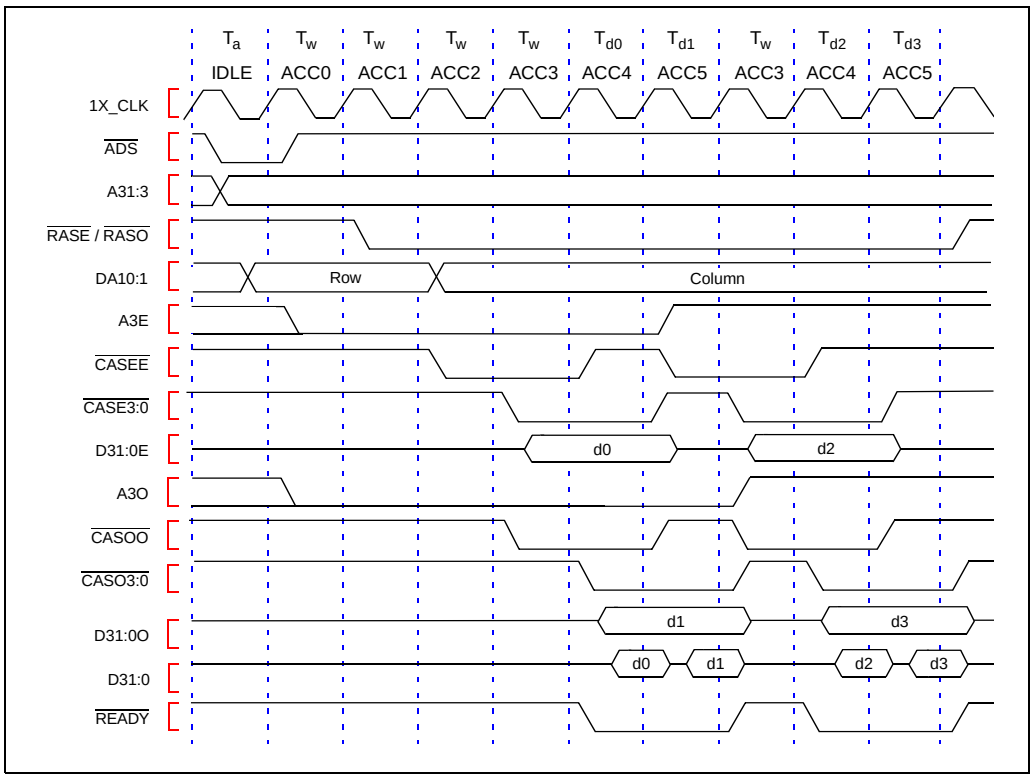

Figure 8. Quad-Word Read Timing Diagram

5.2 Single-Word Read

The ACCESS state machine takes a slightly different path when a read request is aligned on an odd word boundary. Figure 9 shows the state diagram for a single-word read; Figure 10 shows the timing diagram.

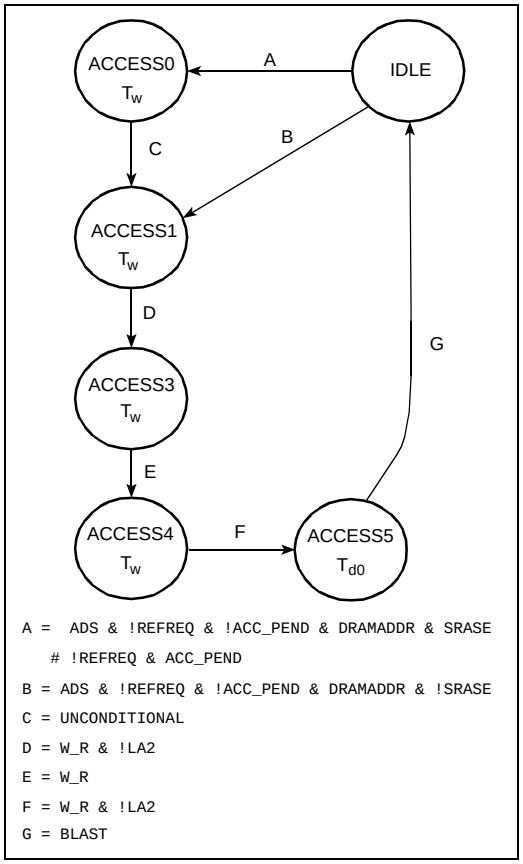

Figure 9. Single-Word Read State Diagram (A2 = 1)

From the IDLE state, the machine enters the ACCESS0 state due to a processor request or a pending processor request. At the end of the IDLE state, the A3EVEN and A3ODD state machines are loaded with the processor's address A3 and the ODDACCESS state machine is loaded with the processor's address A2. $\overline{MUX}$ is deasserted in the IDLE state, which selects the row address.

At the end of the ACCESS0 state, $\overline{RASO}$ is asserted. The machine then proceeds to the ACCESS1 state.

At the end of ACCESS1, $\overline{MUX}$ is asserted. This causes the column address to be selected. $\overline{CASOO}$ is asserted. The PENDING state machine is reset before the machine proceeds to the ACCESS3 state.

At the end of the ACCESS3 state, $\overline{CASOB}$3:0 are asserted if $\overline{CASOO}$ and the respective Byte Enable signals from the processor are asserted. The machine then proceeds to ACCESS4 state.

At the end of the ACCESS4 state, $\overline{CASOO}$ is deasserted and the machine proceeds to the ACCESS5 state.

The ACCESS5 state is the data cycle for the read access. $\overline{CASOB}$3:0 are deasserted. This is primarily because $\overline{CASOO}$ is sampled deasserted. The machine then proceeds to the IDLE state while deasserting $\overline{RASO}$.

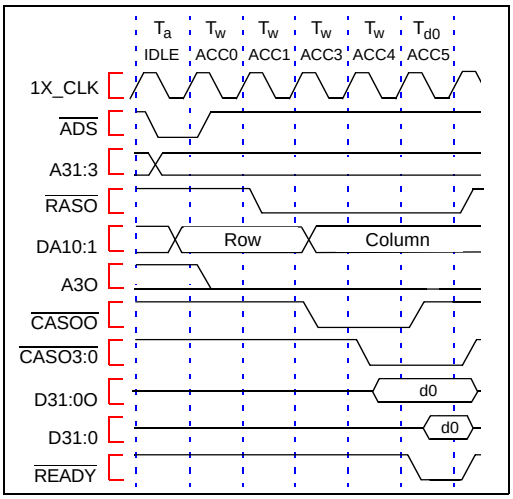

Figure 10. Single-Word Read Timing Diagram (A2 = 1)

5.3 Quad-Word Write

Figure 11 shows the state diagram for a quad-word write. This state diagram also shows the state machine paths for triple-, double-, and single-word writes. Single-word writes which are aligned on odd word boundaries use a different path, therefore, a different example is used to explain the state machine path.

From the IDLE state, the machine enters the ACCESS0 state due to a processor request or a pending processor request. At the end of the IDLE state, the A3EVEN and A3ODD state machines are loaded with the processor's

address A3, and the ODDACCESS state machine is loaded with the processor's address A2. $\overline{MUX}$ is deasserted in the IDLE state, therefore, which selects the row address.

At the end of the ACCESS0 state, $\overline{RASE}$ and $\overline{RASO}$ are asserted. The machine then proceeds to the ACCESS1 state.

At the end of the ACCESS1 state, $\overline{MUX}$ and $\overline{CASEE}$ are asserted. Asserting $\overline{MUX}$ causes the column address to be selected. From ACCESS1, the machine enters the ACCESS2 state.

At the end of the ACCESS2 state $\overline{CASEE}$ is deasserted. $\overline{CASEB}$3:0 are asserted if $\overline{CASEE}$ and the respective Byte Enable signals from the processor are asserted. The machine then proceeds to the ACCESS3 state.

The ACCESS3 state is the first or third data cycle (T_{d0} or T_{d2}) for write accesses which are aligned on even word boundaries (A2 = 0). At the end of the ACCESS3 state, $\overline{CASEB}$3:0 are deasserted. This is because $\overline{CASEE}$ is sampled deasserted. $\overline{CASOO}$ is also asserted if $\overline{BLAST}$ is deasserted. From ACCESS3, the machine can proceed to either the ACCESS4 state or the IDLE state. If $\overline{BLAST}$ is asserted, the machine proceeds to the IDLE state, otherwise to the ACCESS4 state.

At the end of the ACCESS4 state, $\overline{CASOO}$ is deasserted. $\overline{CASOB}$3:0 are asserted if $\overline{CASOO}$ and the respective Byte Enable signals from the processor are asserted. The machine then proceeds to the ACCESS5 state.

The ACCESS5 state is the second or fourth data cycle (T_{d1}/T_{d3}) for write accesses which are aligned on even word boundary (A2 = 0). At the end of ACCESS5, $\overline{CASEE}$ is reasserted. $\overline{CASOB}$3:0 are deasserted. This is because $\overline{CASOO}$ is sampled deasserted. From ACCESS5, the machine can proceed to either the ACCESS2 state or the IDLE state. If $\overline{BLAST}$ is asserted, the machine proceeds to the IDLE state, otherwise to the ACCESS2 state.

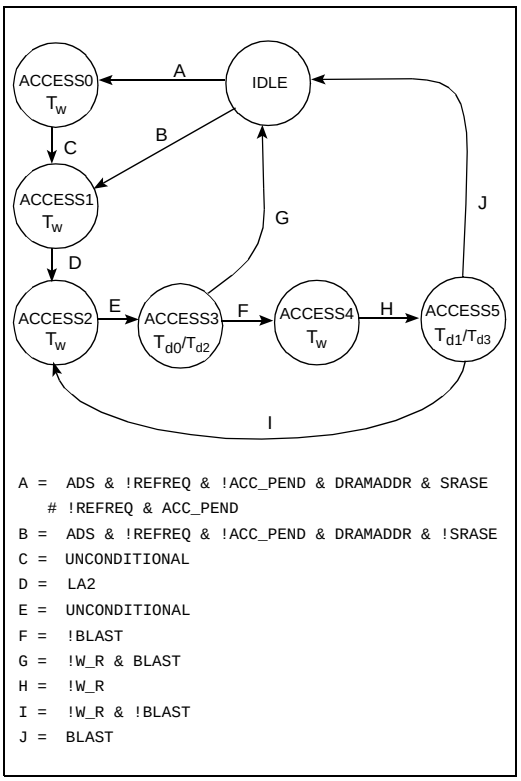

Figure 11. Quad-Word Write State Diagram

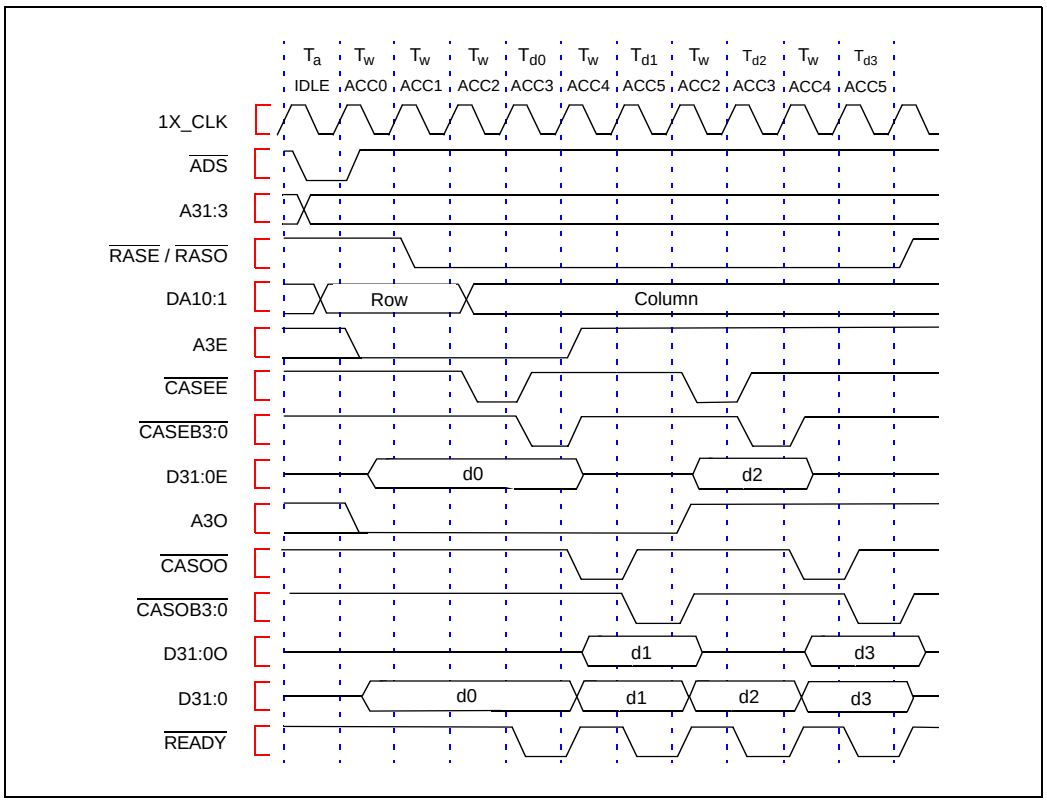

Figure 12. Quad-Word Write Timing Diagram

5.4 Single-Word Write

The ACCESS state machine takes a slightly different path when the write request is aligned on an odd word boundary. Figure 13 shows the state diagram for a single-word write; Figure 14 shows the timing diagram.

From the IDLE state, the machine enters the ACCESS0 state due to a processor request or a pending processor request. At the end of the IDLE state, the A3EVEN and A3ODD state machines are loaded with the processor's address A3, and the ODDACCESS state machine is loaded with the processor's address A2.

At the end of ACCESS0 state, $\overline{RASO}$ is asserted. The machine then proceeds to the ACCESS1 state.

At the end of ACCESS1, $\overline{MUX}$ is asserted. This causes the column address to be selected. $\overline{CASOO}$ is also asserted. From ACCESS1, the machine enters ACCESS4 state.

At the end of the ACCESS4 state, $\overline{CASOB}$3:0 are asserted if $\overline{CASOO}$ and the respective Byte Enable signals from the processor are asserted. $\overline{CASOO}$ is deasserted at the end of ACCESS4. The machine then proceeds to ACCESS5 state.

The ACCESS5 state is the data cycle (T_{d0}) for the write access which is aligned on odd word boundary (A2 = 1). At the end of ACCESS5, $\overline{CASOB}$3:0 are deasserted. The machine then proceeds to the IDLE state.

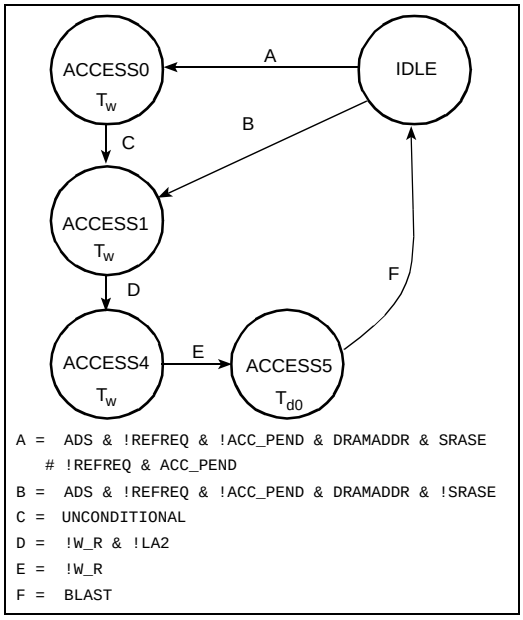

Figure 13. Single-Word Write State Diagram (A2 = 1)

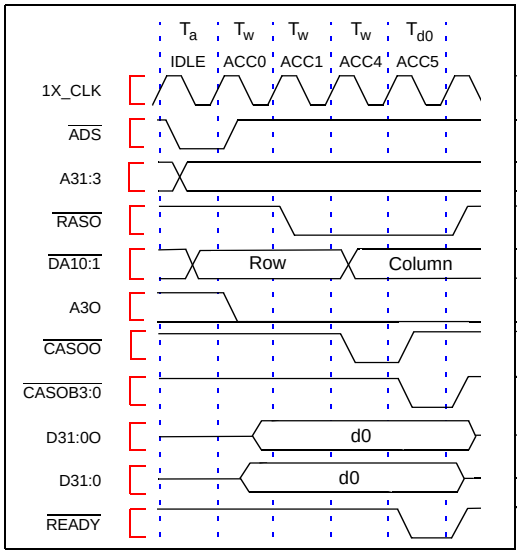

Figure 14. Single-Word Write Timing Diagram (A2 = 1)

5.5 Refresh Cycles

The refresh counter requests a DRAM refresh every 7.8 µs. One bank is refreshed at a time in alternation. The ACCESS state machine sequences the refresh and based on the state of the RFEVENBK state machine, either the even or the odd bank is refreshed. The following text assumes the even bank is to be refreshed, for example the RFEVENBK state machine is active. The odd bank is refreshed in a similar manner when the RFEVENBK state machine is inactive.

Figure 15 shows the refresh state diagram. From the IDLE state, the machine enters the REFRESH0 state if $\overline{\text{REFREQ}}$ is asserted. At the end of REFRESH0, $\overline{\text{CASEE}}$ is asserted. The counter is also reloaded, which deasserts $\overline{\text{REFREQ}}$. Counting resumes on the next clock edge. The machine then proceeds to the REFRESH1 state.

At the end of the REFRESH1 state, $\overline{\text{CASEB}}$3:0 are asserted. $\overline{\text{CASEB}}$3:0 are asserted because $\overline{\text{CASEE}}$ is sampled asserted. The machine then proceeds to the REFRESH2 state.

At the end of the REFRESH2 state, $\overline{\text{RASE}}$ is asserted while $\overline{\text{CASEE}}$ is deasserted. The machine then proceeds to the REFRESH3 state.

At the end of the REFRESH3 state, $\overline{\text{CASEB}}$3:0 are deasserted. This is because $\overline{\text{CASEE}}$ is sampled deasserted. The machine then proceeds to REFRESH4 and REFRESH5 state.

At the end of REFRESH5, $\overline{\text{RASE}}$ is deasserted. The machine then proceeds to the IDLE state

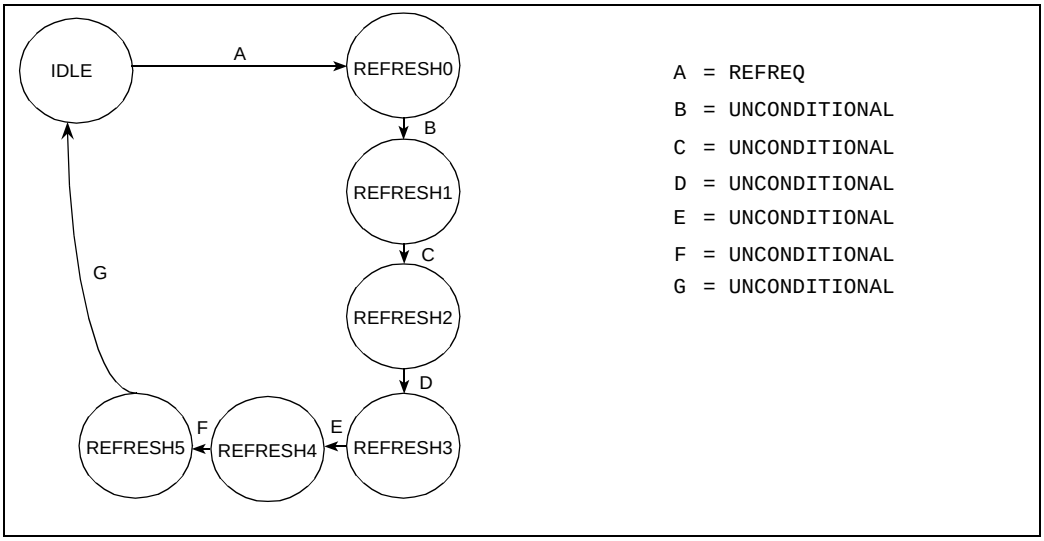

Figure 15. Refresh State Diagram

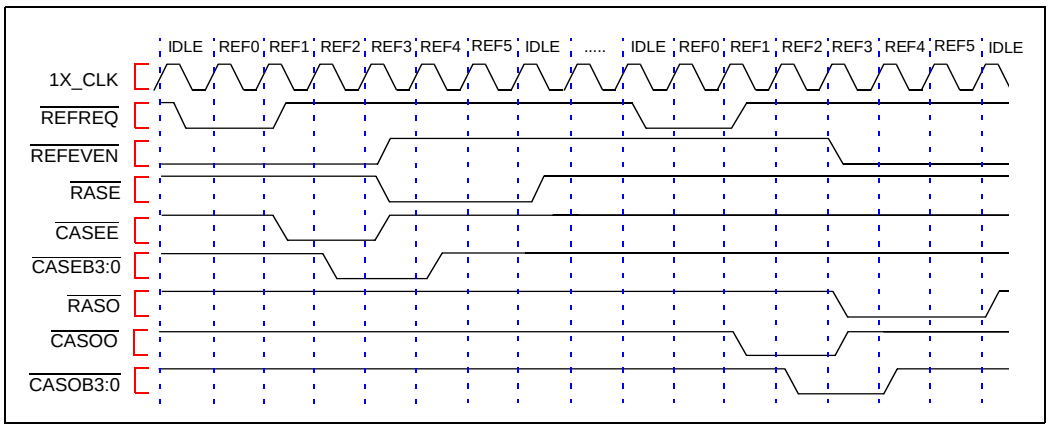

Figure 16. Refresh Timing Diagram

6.0 CONCLUSION

In conclusion, this application note describes a DRAM controller for use with i960® CF 40 MHz microprocessors. This DRAM Controller was built and tested for validation purposes. The PLD equations which were used to build and test the prototype design were created in ABEL. All timing analysis was verified with Timing Designer. Schematics were created with OrCAD. The timing analysis, schematics and PLD files are available through Intel's America's Application Support BBS, at (916) 356-3600.

7.0 RELATED INFORMATION

This application note is one of four that are related to DRAM controllers for the i960 processors. The following table shows the documents and order numbers:

Document Name	App. Note #	Order #
DRAM Controller for the 33, 25, and 16 MHz i960® CA/CF Microprocessors	AP-703	272627
DRAM Controller for the i960® Jx Microprocessors	AP-712	272674
Simple DRAM Controller for 25/16 MHz i960® CA/CF Microprocessors	AP-704	272628

To receive these documents or any other available Intel literature, contact:

Intel Corporation
Literature Sales
P.O. Box 7641
Mt. Prospect IL 60056-7641
1-800-879-4683

To receive files that contain the timing analysis, schematics and PLD equations for this and the other DRAM controller application notes, contact:

Intel Corporation
America's Application Support BBS
916-356-3600

APPENDIX A
PLD EQUATIONS

Table A-1 contains the PLD equations which were used to build and test the prototype design. Table A-2 defines signal and product term allocation. The PLD equations were created in ABEL as a device-independent design. Using the ABEL software*, a PDS file was created and subsequently imported into PLDSHELL software*. PLDSHELL was used to incorporate the design into the Altera EPX780 FLEXlogic PLD*. PLDSHELL was also used to create the JEDEC file, and to simulate the design. In addition, this appendix contains a table listing the number of product terms used by each macrocell.

This DRAM controller does not use the $\overline{\text{APK\_ACTIVE}}$ signal.

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 1 of 19)

```
Module          CX40T
Title           'DRAM Controller for 40MHz
Source File     CX40T.ABL
Revision        Rev 0.0
Date            11/17/94
Designer        Sailesh Bissessur
                Intel i960 Applications Engineering'
"-------------------------------------------------------------------------
" 2-Way Interleaved DRAM controller for the 960CF 40MHz.
" This design also contains logic for FLASH, HEX DISPLAY, and Software Reset
"       DRAM            -  0xA0000000
"       FLASH           -  0xFFFE0000
"       HEX DISPLAY     -  0xB8000000
"       SW Reset        -  0xB0000000
"-------------------------------------------------------------------------
"        Uxx     device  'iFX780_132';
" inputs
        CLK1            PIN; " 1x clock
        CLK2            PIN;

        A2              PIN; " Address A2
        !EXTRST         PIN; " External Reset
        !CPUWAIT        PIN; " Processor Wait
        !ADS            PIN; " Address Strobe
        !BLAST          PIN; " Burst Last
        !W_R            PIN; " Read/Write
        A31             PIN; " Address A31
        A30             PIN; " Address A30
        A29             PIN; " Address A29
        A28             PIN; " Address A28
        A27             PIN; " Address A27
        DCLK1           PIN; " Delayed Clock
        A3              PIN; " Address A3
        !BE3            PIN; " Byte Enable 3
        !BE2            PIN; " Byte Enable 2
        !BE1            PIN; " Byte Enable 1
        !BE0            PIN; " Byte Enable 0
        !APK_ACTIVE     PIN; " Indicate presence of ApLink
```

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 2 of 19)

```
" outputs
        !LA2            PIN  istype 'reg'; " latched A2
        Q3              PIN  istype 'reg'; " m/c bit3
        Q2              PIN  istype 'reg'; " m/c bit2
        !RDEN           PIN  istype 'com'; " enables data mux '257s
        !SELA           PIN  istype 'reg'; " selects even odd data
        !SELB           PIN  istype 'reg'; " selects even odd data
        !READY          PIN  istype 'reg'; " Processor READY
        Q1              PIN  istype 'reg'; " m/c bit1
        Q0              PIN  istype 'reg'; " m/c bit0
        !ACC_PEND       PIN  istype 'reg'; " access pending indicator
        !RASO           PIN  istype 'reg'; " Odd RAS
        A3E             PIN  istype 'reg'; " Even Address Counter
        !REFEVEN        PIN  istype 'reg'; " which bank to refresh
        !CASEE          PIN  istype 'reg'; " Pipelined Even CAS
        !CASOO          PIN  istype 'reg'; " Pipelined Odd CAS
        A3O             PIN  istype 'reg'; " Odd Address Counter
        !WAIT           PIN  istype 'com'; " wait state indicator
        !RASE           PIN  istype 'reg'; " Even RAS
        !MUX            PIN  istype 'reg'; " Selects Row/Column Address
        !CASEB0         PIN  istype 'reg'; " Byte 0 Even CAS
        !CASEB1         PIN  istype 'reg'; " Byte 1 Even CAS
        !CASEB2         PIN  istype 'reg'; " Byte 2 Even CAS
        !CASEB3         PIN  istype 'reg'; " Byte 3 Even CAS
        !CASOB0         PIN  istype 'reg'; " Byte 0 Odd CAS
        !CASOB1         PIN  istype 'reg'; " Byte 1 Odd CAS
        !CASOB2         PIN  istype 'reg'; " Byte 2 Odd CAS
        !CASOB3         PIN  istype 'reg'; " Byte 3 Odd CAS
        S3              PIN  istype 'reg'; " Refresh Counter 1 bit 3
        S2              PIN  istype 'reg'; " Refresh Counter 1 bit 2
        S1              PIN  istype 'reg'; " Refresh Counter 1 bit 1
        S0              PIN  istype 'reg'; " Refresh Counter 1 bit 0
        T3              PIN  istype 'reg'; " Refresh Counter 2 bit 3
        T2              PIN  istype 'reg'; " Refresh Counter 2 bit 2
        T1              PIN  istype 'reg'; " Refresh Counter 2 bit 1
        T0              PIN  istype 'reg'; " refresh Counter 2 bit 0
        !REFREQ         PIN  istype 'com'; " Refresh Required
        !FLASHCS        PIN  istype 'reg'; " FLASH Chip Select
        !FLASHRD        PIN  istype 'reg'; " FLASH OE
        !FLASHWR        PIN  istype 'com'; " FLASH WE
        !XCROE          PIN  istype 'reg'; " XCR OE control
        !XCRDIR         PIN  istype 'com'; " XCR DIR control
        !SWRST          PIN  istype 'reg'; " SW Reset Indicator
        !TRIGRST        PIN  istype 'reg'; " Triggers the 7705
        !RESET          PIN  istype 'reg'; " System Reset
        !WRE            PIN  istype 'com'; " Odd Bank WE
        !WRO            PIN  istype 'com'; " Even Bank WE
        !SRASE          PIN  istype 'reg'; " Shifted RASE
        LED_LAT         PIN  istype 'reg'; " Hex Display Pulse
"
C = .C.;
X = .X.;

"
```

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 3 of 19)

```
CYCLE       = [Q3,Q2,Q1,Q0];
ODDACCESS   = [LA2];
BANKSELA    = [SELA];
BANKSELB    = [SELB];
PENDING     = [ACC_PEND];
RDY         = [READY];
RASEVEN     = [RASE];
RASODD      = [RASO];
CASPIPE     = [CASEE];
CASPIPO     = [CASOO];
ADDRMUX     = [MUX];
A3EVEN      = [A3E];
A3ODD       = [A3O];
RFEVENBK    = [REFEVEN];
CASE_B0     = [CASEB0];
CASE_B1     = [CASEB1];
CASE_B2     = [CASEB2];
CASE_B3     = [CASEB3];
CASO_B0     = [CASOB0];
CASO_B1     = [CASOB1];
CASO_B2     = [CASOB2];
CASO_B3     = [CASOB3];
REFCT2 = [T3,T2,T1,T0];
REFCT1 = [S3,S2,S1,S0];
DRAMADDR  = (A31 & !A30 &  A29 & !A28 & !A27);
FLASHADDR = (A31 &  A30 &  A29 &  A28 &  A27);
SWRSTADDR = (A31 & !A30 &  A29 &  A28 & !A27);
LEDADDR   = (A31 & !A30 &  A29 &  A28 &  A27);

"
ASSERT   = ^b1;
DEASSERT = ^b0;

Z0       = ^b0000;
Z1       = ^b0001;
Z2       = ^b0010;
Z3       = ^b0011;
Z4       = ^b0100;
Z5       = ^b0101;
Z6       = ^b0110;
Z7       = ^b0111;
Z8       = ^b1000;
Z9       = ^b1001;
Z10      = ^b1010;
Z11      = ^b1011;
Z12      = ^b1100;
Z13      = ^b1101;
Z14      = ^b1110;
Z15      = ^b1111;
```

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 4 of 19)

```
IDLE          = ^b0000;
ACCESS0       = ^b0001;
ACCESS1       = ^b0010;
ACCESS2       = ^b0011;
ACCESS3       = ^b0100;
ACCESS4       = ^b0101;
ACCESS5       = ^b0110;
ACCESS6       = ^b0111; “this state is never entered
ACCESS7       = ^b1000; “this state is never entered
REFRESH0      = ^b1001;
REFRESH1      = ^b1010;
REFRESH2      = ^b1011;
REFRESH3      = ^b1100;
REFRESH4      = ^b1101;
REFRESH5      = ^b1110;
REFRESH6      = ^b1111; “this state is never entered

"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
"Holds state of A2 of the processor
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
state_diagram ODDACCESS
                state ASSERT:
                        if((CYCLE == IDLE) & A2) then DEASSERT
                else
                        ASSERT;

                state DEASSERT:
                        if((CYCLE == IDLE) & !A2) then ASSERT
                else
                        DEASSERT;
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
"Even byte 0 CAS
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
state_diagram CASE_B0
                state ASSERT:
                        if(!Q3 & !CASEE) then DEASSERT
                else
                        if(Q3 & !CASEE) then DEASSERT
                else
                        ASSERT;

                state DEASSERT:
                        if(!Q3 & W_R & WAIT & CASEE & BE0) then ASSERT
                else
                        if(!Q3 & W_R & !WAIT & CASEE & BE0 & !BLAST) then ASSERT
                else
                        if(!Q3 & !W_R & CASEE & BE0) then ASSERT
                else
                        if(Q3 & CASEE) then ASSERT
                else
                        DEASSERT;
```

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 5 of 19)

```
""""""
```

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 6 of 19)

```
"""""""
```

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 7 of 19)

```
"""""""
```

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 8 of 19)

```
"""""""
```

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 9 of 19)

```
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
"Selects even or odd data
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
state_diagram BANKSELA
                state ASSERT:
                        if(CYCLE == ACCESS4) then DEASSERT
                else
                        if((CYCLE == IDLE) & W_R & A2) then DEASSERT
                else
                        ASSERT;

                state   DEASSERT:
                        if((CYCLE == ACCESS3) & W_R) then ASSERT
                else
                        if((CYCLE == IDLE) & W_R & !A2) then ASSERT
                else
                        DEASSERT;

"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
"Selects even or odd data
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
state_diagram BANKSELB
                state ASSERT:
                        if(CYCLE == ACCESS4) then DEASSERT
                else
                        if((CYCLE == IDLE) & W_R & A2) then DEASSERT
                else
                        ASSERT;

                state   DEASSERT:
                        if((CYCLE == ACCESS3) & W_R) then ASSERT
                else
                        if((CYCLE == IDLE) & W_R & !A2) then ASSERT
                else
                        DEASSERT;

"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
"Generates READY to the processor
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
state_diagram RDY
                state ASSERT:
                        if((CYCLE == ACCESS4) & W_R & BLAST) then DEASSERT
                else
                        if((CYCLE == ACCESS5)) then DEASSERT
                else
                        if((CYCLE == ACCESS3)) then DEASSERT
                else
                        ASSERT;

                state DEASSERT:
                        if((CYCLE == ACCESS2) & !W_R) then ASSERT
                else
                        if((CYCLE == ACCESS3) & W_R & LA2) then ASSERT
                else
                        if((CYCLE == ACCESS4) & W_R & !LA2) then ASSERT
                else
                        if((CYCLE == ACCESS4) & !W_R) then ASSERT
                else
                        DEASSERT;
```

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 10 of 19)

```
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
"Even RAS
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
state_diagram RASEVEN
                state ASSERT:
                        if((CYCLE == ACCESS3) & !W_R & BLAST) then DEASSERT
                else
                        if((CYCLE == ACCESS4) & W_R & BLAST & LA2) then DEASSERT
                else
                        if((CYCLE == ACCESS5) & BLAST) then DEASSERT
                else
                        if((CYCLE == REFRESH5)) then DEASSERT
                else
                        ASSERT;

                state DEASSERT:
                         if((CYCLE == IDLE) & ADS & !REFREQ & !ACC_PEND
                             & DRAMADDR & !SRASE) then ASSERT
                else
                        if((CYCLE == ACCESS0)) then ASSERT
                else
                        if((CYCLE ==  REFRESH2) & REFEVEN) then ASSERT
                else
                        DEASSERT;
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
"Odd RAS
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
state_diagram RASODD
                state ASSERT:
                        if((CYCLE == ACCESS3) & !W_R & BLAST) then DEASSERT
                else
                        if((CYCLE == ACCESS4) & W_R & BLAST & LA2) then DEASSERT
                else
                        if((CYCLE == ACCESS5) & BLAST) then DEASSERT
                else
                        if((CYCLE == REFRESH5)) then DEASSERT
                else
                        ASSERT;

                state DEASSERT:
                            if((CYCLE == IDLE) & ADS & !REFREQ & !ACC_PEND
                               & DRAMADDR & !SRASE) then ASSERT
                else
                        if((CYCLE == ACCESS0))  then ASSERT
                else
                        if((CYCLE == REFRESH2) & !REFEVEN) then ASSERT
                else
                        DEASSERT;
```

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 11 of 19)

```
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
"Pipelined Even CAS
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
state_diagram CASPIPE
                state ASSERT:
                        if((CYCLE == ACCESS2) & !W_R) then DEASSERT
                else
                        if((CYCLE == ACCESS3) & W_R) then DEASSERT
                else
                        if((CYCLE == ACCESS5) & BLAST & W_R) then DEASSERT
                else
                        if((CYCLE == REFRESH2)) then DEASSERT
                else
                        ASSERT;

                state DEASSERT:
                        if((CYCLE == ACCESS1) & LA2) then ASSERT
                else
                        if((CYCLE == ACCESS4) & W_R & LA2 & !BLAST) then ASSERT
                else
                        if((CYCLE == ACCESS5) & !W_R & !BLAST) then ASSERT
                else
                        if((CYCLE == REFRESH0) & REFEVEN) then ASSERT
                else
                        DEASSERT;
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
"Pipelined Odd CAS
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
state_diagram  CASPIPO
                state ASSERT:
                        if((CYCLE == ACCESS4)) then DEASSERT
                else
                        if((CYCLE == REFRESH2)) then DEASSERT
                else
                        ASSERT;

                state DEASSERT:
                        if((CYCLE == ACCESS2) & W_R & LA2 & !BLAST) then ASSERT
                else
                        if((CYCLE == ACCESS3) & !W_R & LA2 & !BLAST) then ASSERT
                else
                        if((CYCLE == ACCESS1) & !LA2) then ASSERT
                else
                        if((CYCLE == ACCESS5) & !BLAST & W_R) then ASSERT
                else
                        if((CYCLE == REFRESH0) & !REFEVEN) then ASSERT
                else
                        DEASSERT;
```

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 12 of 19)

```
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
"Even address counter
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
state_diagram A3EVEN
                  state DEASSERT:
                          if((CYCLE == IDLE) &  A3) then ASSERT
                  else
                          if((CYCLE == ACCESS4)) then ASSERT
                  else
                          DEASSERT;

                  state ASSERT:
                          if((CYCLE == IDLE) & !A3) then DEASSERT
                  else
                          if((CYCLE == ACCESS4)) then DEASSERT
                  else
                          ASSERT;
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
"Odd address counter
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
state_diagram A3ODD
                  state DEASSERT:
                          if((CYCLE == IDLE) &  A3) then ASSERT
                  else
                          if((CYCLE == ACCESS5)) then ASSERT
                  else
                          DEASSERT;

                  state ASSERT:
                          if((CYCLE == IDLE) & !A3)  then DEASSERT
                  else
                          if((CYCLE == ACCESS5)) then DEASSERT
                  else
                          ASSERT;
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
"Main DRAM state machine - ACCESS state machine
"""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
state_diagram CYCLE
                  state IDLE:
                       if(ADS & !REFREQ & !ACC_PEND & DRAMADDR &  SRASE) then ACCESS0
                  else
                       if(ADS & !REFREQ & !ACC_PEND & DRAMADDR & !SRASE) then ACCESS1
                  else
                          if(!REFREQ & ACC_PEND) then ACCESS0
                  else
                          if(REFREQ) then REFRESH0
                  else
                          IDLE;

                  state ACCESS0:
                          goto ACCESS1;

                  state ACCESS1:
                          if(W_R & !LA2) then ACCESS3
                  else
                          if(!W_R & !LA2) then ACCESS4
                  else
                          ACCESS2;

                  state ACCESS2:
                          goto ACCESS3;
```

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 13 of 19)

```
                state ACCESS3:
                        if(!W_R & BLAST) then IDLE
                else
                        ACCESS4;

                state ACCESS4:
                        if(W_R & LA2 & BLAST) then IDLE
                else
                        ACCESS5;

                state ACCESS5:
                        if(BLAST) then IDLE
                else
                        if(!W_R & !BLAST) then ACCESS2
                else
                        if(W_R & !BLAST) then ACCESS3
                else
                        IDLE;

                state ACCESS6:
                        goto IDLE;

                state ACCESS7:
                        goto REFRESH0;

                state REFRESH0:
                        goto REFRESH1;

                state REFRESH1:
                        goto REFRESH2;

                state REFRESH2:
                        goto REFRESH3;

                state REFRESH3:
                        goto REFRESH4;

                state REFRESH4:
                        goto REFRESH5;

                state REFRESH5:
                        goto IDLE;

                state REFRESH6:
                        goto IDLE;
""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
"Row/Column address select
""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
state_diagram ADDRMUX
                state ASSERT:
                        if(!RASE) then DEASSERT
                else
                        ASSERT;

                state DEASSERT:
                        if(RASE) then ASSERT
                else
                        DEASSERT;
```

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 14 of 19)

```
"""""""
```

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 15 of 19)

```
state Z11:
        if(Q3) then Z15
else
        Z10;

state Z12:
        if(Q3) then Z15
else
        Z11;

state Z13:
        if(Q3) then Z15
else
        Z12;

state Z14:
        if(Q3) then Z15
else
        Z13;

state Z15:
        if(Q3) then Z15
else
        Z14;
```

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 16 of 19)

```
"""""""
```

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 17 of 19)

```
state Z8:
        if(Q3) then Z15
else
        if(!Q3 & (REFCT1 == Z0)) then Z7;
else
        Z8;

state Z9:
        if(Q3) then Z15
else
        if(!Q3 & (REFCT1 == Z0)) then Z8;
else
        Z9;

state Z10:
        if(Q3) then Z15
else
        if(!Q3 & (REFCT1 == Z0)) then Z9;
else
        Z10;

state Z11:
        if(Q3) then Z15
else
        if(!Q3 & (REFCT1 == Z0)) then Z10;
else
        Z11;

state Z12:
        if(Q3) then Z15
else
        if(!Q3 & (REFCT1 == Z0)) then Z11;
else
        Z12;

state Z13:
        if(Q3) then Z15
else
        if(!Q3 & (REFCT1 == Z0)) then Z12;
else
        Z13;

state Z14:
        if(Q3) then Z15
else
        if(!Q3 & (REFCT1 == Z0)) then Z13;
else
        Z14;

state Z15:
        if(Q3) then Z15
else
        if(!Q3 & (REFCT1 == Z0)) then Z14;
else
        Z15;
```

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 18 of 19)

```
"
" Equations
"
EQUATIONS

[Q3,Q2,Q1,Q0,!SELA,!SELB,!READY,!LA2,!ACC_PEND].clk = CLK1;
[Q3..Q0].RE = RESET;

[!LA2,!ACC_PEND,!READY,!SELA,!SELB].PR = RESET;
"
"Indicates wait state cycles
"
WAIT =    (CYCLE == ACCESS0) & W_R
        # (CYCLE == ACCESS1) & W_R
        # (CYCLE == ACCESS2) & W_R
        # (CYCLE == ACCESS3) & W_R;

[!MUX,!RASE,!RASO,!CASEE,!CASOO,A3E,A3O,!REFEVEN].clk = CLK1;
[!MUX,!RASE,!RASO,!CASEE,!CASOO,A3E,A3O,!REFEVEN].pr = RESET;

[!CASEB0,!CASEB1,!CASEB2,!CASEB3,!CASOB0,!CASOB1,!CASOB2,!CASOB3].clk = CLK1;

[T3,T2,T1,T0,S3,S2,S1,S0].clk = CLK1;
[T3,T2,T1,T0,S3,S2,S1,S0].pr = RESET;
"
"Refresh required indicator
"
REFREQ = !T3 & !T2 & !T1 & !T0 & !S3 & !S2 & !S1 & !S0;
"
"FLASH Chip Select
"
FLASHCS :=    ADS & FLASHADDR & !APK_ACTIVE
           # !ADS & !BLAST & FLASHCS;
"
"FLASH OE control
"
FLASHRD = FLASHCS & W_R;
"
"XCR OE control
"
XCROE :=   FLASHCS & !BLAST & !APK_ACTIVE
         # !ADS & LEDADDR & !BLAST;
"
"XCR DIR control
"
XCRDIR = W_R;
"
"Software reset indicator
"
SWRST :=    ADS & SWRSTADDR
         # !ADS & !BLAST & SWRST;
"
"Triggers the 7705
"
TRIGRST := TRIGRST;
TRIGRST.RE = SWRST;
```

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 19 of 19)

```
"
"Pulse the HEX DISPLAY
"
LED_LAT  := !ADS & LEDADDR & XCROE & !BLAST;
"
"Latched RASE or RASO
"
SRASE := RASE # RASO;
"
"DRAM data path control while reading
"
RDEN = !Q3 &  W_R & RASE;
"
" Even DRAM data path control while writing
"
WRE  = !Q3 & !W_R & RASE;
"
"Odd DRAM data path control while writing
"
WRO  = !Q3 & !W_R & RASE;

[!FLASHCS,!XCROE,!SWRST,!TRIGRST,LED_LAT,SRASE].clk = CLK1;
[!FLASHCS,!XCROE,!SWRST,!TRIGRST].pr = RESET;
LED_LAT.RE = RESET;
"
"Latched external reset
"
RESET := EXTRST;
RESET.CLK = CLK1;

" Test vectors

end CX40T
```

Table A-2. Signal and Product Term Allocation

OUTPUTS		BURIED MACROCELLS	
Signal	**Product Terms**	**Signal**	**Product Terms**
$\overline{\text{RASE}}$	7	$\overline{\text{CASEE}}$	10
$\overline{\text{RASO}}$	7	$\overline{\text{CASOO}}$	9
$\overline{\text{READY}}$	6	Q3	3
A3E	3	Q2	8
A3O	3	Q1	9
$\overline{\text{SELA}}$	4	Q0	9
$\overline{\text{MUX}}$	1	$\overline{\text{ACC\_PEND}}$	5
$\overline{\text{RDEN}}$	1	$\overline{\text{LA2}}$	5
$\overline{\text{CASEB3}}$	3	$\overline{\text{WAIT}}$	3
$\overline{\text{CASEB2}}$	3	$\overline{\text{REFEVEN}}$	5
$\overline{\text{CASEB1}}$	3	T3	2
$\overline{\text{CASEB0}}$	3	T2	8
$\overline{\text{CASOB3}}$	5	T1	7
$\overline{\text{CASOB2}}$	5	T0	6
$\overline{\text{CASOB1}}$	5	S3	5
$\overline{\text{CASOB0}}$	5	S2	4
$\overline{\text{FLASHCS}}$	2	S1	3
$\overline{\text{FLASHRD}}$	1	S0	2
$\overline{\text{TRIGRST}}$	1	$\overline{\text{REFREQ}}$	1
$\overline{\text{XCROE}}$	2	$\overline{\text{SWRST}}$	2
$\overline{\text{XCRDIR}}$	1	$\overline{\text{SRASE}}$	1
$\overline{\text{RESET}}$	1		
$\overline{\text{WRE}}$	1		
$\overline{\text{WRO}}$	1		
LED_LAT	1		
$\overline{\text{SELB}}$	4		

S

T

W